

CLAIMS

The following listing of claims replaces all prior versions and listings of claims in the above-referenced application:

- 1 1. (Currently amended) A system comprising:
2 shared system registers, each shared system register including ~~one or more~~ bits
3 defining an access protocol, and one or more bits representing data; and
4 N processors, $N \geq 2$, where N is an integer, each of the N processors accessing
5 the shared system registers, wherein said ~~one or more~~ bits defining the access protocol
6 include ~~one or more~~ bits that define a register access type comprising access modes
7 for each of the N processors.
- 1 2. (Canceled)
- 1 3. (Previously presented) A system, as defined in claim 1, the register
2 access type being selected from a group that includes READ, READ/CLEAR,
3 READ/SET, and READ/WRITE.
- 1 4. (Previously presented) A system, as defined in claim 3, further
2 comprising at least one programmable configuration register operative to encode and
3 store said one or more bits defining the access protocol, each of said at least one
4 programmable configuration register corresponding to one of the shared system
5 registers.
- 1 5. (Previously presented) A system, as defined in claim 4, wherein:
2 each programmable configuration register consists of $N*2$ bits; and
3 the configurable register access types are encoded into 2 bits.
- 1 6. (Currently amended) A system, as defined in claim [3] 1, the
2 access protocol encoded and provided as input signals to a hardware design.

1 7. (Currently amended) A system, as defined in claim [3] 1, the
2 access protocol encoded and selected as a build-time option in a hardware design
3 source code.

1 8. (Currently amended) A system, as defined in claim [3] 1, the
2 access protocol further including an arbitration priority.

1 9. (Previously presented) A system, as defined in claim 8, comprising
2 programmable configuration registers operative to encode and store the access
3 protocol, each programmable configuration register corresponding to one of the
4 shared system registers.

1 10. (Previously presented) A system, as defined in claim 9, wherein:
2 N is 2; and
3 each programmable configuration register includes 5-bits, 2 bits represent the
4 access type of one of the two processors, 2 bits represent the access type of the other
5 of the two processors, and 1 bit represents the arbitration priority.

1 11. (Previously presented) A system, as defined in claim 9, wherein:
2 each programmable configuration register consists of $N \cdot (2 + \text{ceiling}(\log_2 N))$
3 bits; and
4 the access protocol including the four access types are encoded into 2 bits per
5 processor and the arbitration priority encoded into $\text{ceiling}(\log_2 N)$ bits.

1 12. (Previously presented) A system, as defined in claim 8, the access
2 protocol encoded and selected as a build-time option in a hardware design source
3 code.

1 13. (Previously presented) A system, as defined in claim 8, the access
2 protocol encoded and provided as input signals to a hardware design.